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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,148	11/13/2003	Minoru Sudou	S004-5152	8187

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,148	SUDOU, MINORU	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6 and 8-13* is/are rejected.

7)☐ Claim(s) *2-5,7 and 14-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 11/14/2002. It is noted, however, that applicant has not filed a certified copy of the 2002-330847 application as required by 35 U.S.C. 119(b).

Claim Objections

2. Claims 8-17 are objected to because of the following informalities:

Claim 8, line 13, "and one" should be changed to --and the one-- to avoid unclear antecedent basis (see line 11 of claim 8).

Claims 9-17 are objected to because they include the informality of claim 8.

Also in claim 10, "a voltage" should be changed to –the voltage—to avoid unclear antecedent basis (see line 4 of claim 8).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato (JP 64-11413).

With respect to claims 8 and 10, Figure 1 of the Sato reference discloses a circuit, which includes: input terminals (terminal connected to received Vcc and terminal connected to ground

GD); an output terminal (output terminal connected to provide CLR/); a reference voltage generator (1-3) for generating a reference voltage (voltage at the junction node of elements 1-3); a comparator (6) for comparing the reference voltage with a voltage across the input terminals (divider 4-5 divides the voltage across Vcc and ground for providing a divided voltage to the positive terminal of comparator 6, i.e., the voltage at the junction connection of elements 4-5) and for outputting a comparison signal (output of 6); a first output circuit (9-11) for outputting a first signal (CLR/); and a second output circuit (12-17) connected between the output terminal (output provided CLR/) and one of the input terminals (note that element 17 connected between the output terminal and ground GD) for varying a resistance value between the output terminal and the one of the input terminals based on the voltage across the input terminals (i.e., when the value of voltage Vcc changes, then the voltage controls the based of transistor 17 also changes and thus varying the resistance between the output terminal and ground GD).

5. Claims 8 and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohshima (USP 5,268,595).

With respect to claims 8 and 10-13, Figure 5 of the Ohshima reference discloses a circuit, which includes: input terminals (terminal connected to received Vdd and terminal connected to ground GND); an output terminal (OUT11); a reference voltage generator (12) for generating a reference voltage (Vref); a comparator (11a-11b) for comparing the reference voltage with a voltage across the input terminals (divider 13 divides the voltage across Vcc and ground for providing a divided voltage Vm at node 12 to the comparator 11a-11b) and for outputting a comparison signal (signal to gates of Q9 and Q10); a first output circuit (11c which comprises enhancement mode PMOS Q9 and NMOS Q10) for outputting a first signal to the first output

terminal (OUT11, by way of Q11-Q12); and a second output circuit (R23, R22, Q11, Q12) connected between the output terminal (OUT11) and one of the input terminals (note that element R22 connected between the output terminal and ground GND) for varying a resistance value between the output terminal and the one of the input terminals based on the voltage across the input terminals (i.e., the on/off of transistor Q12 causes the impedance between the output terminal OUT11 and ground varying).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima (USP 5,268,595) in view of Sudo (US 2002/0140402).

With respect to claim 1, Figure 5 of the Ohshima reference discloses a circuit, which includes: a first terminal (terminal connected to received Vdd); a second terminal (terminal connected to GND); a voltage dividing circuit (13) for dividing a voltage (VDD) across the first and second terminals; a reference voltage (22); a comparator (11a, 11b) and outputs a comparison signal (the signal connected to gates of Q9 and Q10); a first output circuit (11c) for outputting a first signal (output of 11c); and a second output circuit (R23, R22, Q11, Q12) connected between the output terminal and one of the first and second terminals (note that resistor R23 connected between Vdd and output terminal N21) for outputting a second output signal (at node OUT11) that change in value on the basis of a first signal and a second signal at

the first terminal and the second terminal, respectively (Vdd and ground GND, i.e., when the value of voltage between Vdd and GND changes, then the output of at node OUT11 also changes). The Ohshima reference fails to disclose that the voltage Vdd across the first and second terminals is used from a battery. However, the Sudo reference discloses that a battery is used as the power supply voltage in an integrated circuit in a portable device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit in Figure 5 of the Ohshima reference by using a battery for power supply voltage Vdd for the purpose of using the circuit in portable device such as in cordless phone or cell-phone. Thus this modification meets all the limitations of claim 1.

With respect to claim 6, the modification in Figure 5 shows that the first output circuit (11c) comprises two enhancement mode MOS transistors (Q9 and Q10).

With respect to claim 9, the circuit in Figure 5 of the Ohshima reference as discussed in the 102 rejection of claim 8 above meets all the limitations of this claim except that the voltage Vdd across the first and second terminals is used from a battery. However, the Sudo reference discloses that a battery is used as the power supply voltage in an integrated circuit in a portable device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit in Figure 5 of the Ohshima reference by using a battery for power supply voltage Vdd for the purpose of using the circuit in portable device such as in cordless phone or cell-phone. Thus this modification meets all the limitations of claim 9.

8. Claims 9 is also rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (JP 64-11413) in view of Sudo (US 2002/0140402).

With respect to claim 9, the circuit in Figure 1 of the Sato reference as discussed in the 102 rejection of claim 8 above meets all the limitations of this claim except that the voltage Vdd across the first and second terminals is used from a battery. However, the Sudo reference discloses that a battery is used as the power supply voltage in an integrated circuit in a portable device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit in Figure 1 of the Sato reference by using a battery for power supply voltage Vdd for the purpose of using the circuit in portable device such as in cordless phone or cell-phone. Thus this modification meets all the limitations of claim 9.

Allowable Subject Matter

9. Claims 2-5, 7 and 14-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the informalities set forth above (claims 14-17).

Response to Arguments

10. Applicant's arguments filed on 5/27/05 have been considered but are moot in view of the new ground(s) of rejection.

Also note that applicant argues the Ohshima reference does not disclose a second output circuit as required in the amended claims 1 and 8. However, the Ohshima reference discloses a second output circuit (R23, R22, Q11, Q12) in Figure 5 that meets the requirement of "second output circuit" in the amended claims 1 and 8 as discussed above in the rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 28, 2005

LONG NGUYEN
PRIMARY EXAMINER